Introduction

SR2_Analog_24-bit is an analog conversion board for the *Signal_Ranger_mk2* DSP board. It is optimized for a high signal-to-noise ratio (SNR) and for audio bandwidth applications. It provides two functions:

- 8 analog inputs and 4 analog outputs; they are all 24-bit and have a high SNR.
- 59 general-purpose I/Os arranged as three 16-bit ports and one 11-bit port.
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Note: *Signal_Ranger_mk2's FPGA is used to manage the ADCs and DACs on SR2_Analog_24-bit. To be functional the FPGA must be loaded with a special logic that is different from the factory-default logic implemented in Signal_Ranger_mk2. Any logic implemented in the FPGA of Signal_Ranger_mk2 at power-up that is not the logic designed to manage SR2_Analog_24-bit, including the factory-default logic, has the potential to damage the FPGA and the SR2_Analog_24-bit board. If SR2_Analog_24-bit has been purchased separately from Signal_Ranger_mk2 we recommend to either load the SR2_Analog_24-bit logic, or erase any logic in Flash prior to mating SR2_Analog_24-bit to Signal_Ranger_mk2. The procedure is described in Signal_Ranger_mk2's user manual.*

1 Technical Data

1.1 Analog Inputs

- Number of inputs: 8
- Resolution: 24 bits
- SNR: 109 dB
- Sampling rate: 48.8kHz
- Analog input bandwidth: 0 to 24.4kHz (includes DC)
- Input type: Single Ended
- Dynamic range: +-2V
- Anti-aliasing filter: FIR, group-delay 39 samples
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1.2 Analog Outputs

- Number of outputs: 4
- Resolution: 24 bits
- SNR: 105 dB
- Sampling rate: 48.8kHz
- Analog output bandwidth: 0 to 24.4kHz
- Output type: Single Ended
- Dynamic range: +-2V
- Source/Sink ability: 10mA
- Anti-aliasing filter: IIR, group-delay 29 samples

1.3 General-Purpose I/Os

- Number of I/Os: 59 (three 16-bit port and one 11-bit port).
- Configurability: All I/Os individually configurable as input or output.
- IO level: 3.3V CMOS (5V-tolerant inputs)